I CLAIM

1. An image processor arranged in operation to generate an interpolated video signal from a received video signal representative of an image, said image processor comprising

- a register store coupled to

- a control processor, said register store being arranged in operation to receive said video signal and to provide pixels of said received video signal, under control of said control processor, to an interpolator,

- said interpolator being coupled to said register store and arranged in operation to generate said interpolated video signal by interpolating said pixels provided by said register store, wherein said control processor controls in operation said register store to provide pixels to said interpolator to interpolate features of said image having both a vertical and a horizontal component.

2. An image processor as claimed in Claim 1, wherein said shift register has a plurality of register elements, selected register elements being connected to said interpolator to provide said pixels of said received video signal for interpolation, each of said register elements being arranged to store a pixel of said received video signal and each is connected to a plurality of other register elements and is configurable under control of said control processor to feed the pixel stored in said register element to one or other of said other shift registers in accordance with a temporal reference.

3. An image processor as claimed in Claims 2, wherein said shift register comprises a plurality of delay stores coupled in series, a first of the delay stores being arranged to receive said received video signal, each delay store being arranged to delay said received video signal by an amount corresponding to one line of said received video signal, and an output of each of said delay stores is arranged to feed said delayed received video signal to a corresponding register element.

4. An image processor as claimed in Claim 1, wherein said control processor is arranged in operation to detect said feature of said image having both vertical and

horizontal components, said control processor operating to control the configuration of said register elements to provide the input pixels associated with said feature to said interpolator.

5. An image processor as claimed in Claim 3, wherein said plurality of register elements are arranged with reference to a plurality of columns, each column having at least two rows of register elements, the plurality of other register elements to which each shift register is connected being at least two of the register element of the next column, the register element one row above of the next column, and the register element one row below of the next column.

6. An image processor as claimed in Claim 5, wherein the pixels stored in each of the shift registers on a substantially diagonal line formed on said column and row arrangement of said plurality of register elements are coupled to said interpolator, the interpolation of the received video signal for the feature having vertical and horizontal components being effected for the pixels stored in the diagonal line of shift registers.

7. An image processor as claimed in Claim 3, comprising

- a clock which is arranged to provide said temporal reference to said register elements, wherein said temporal reference is derived with respect to a rate of receiving said pixels of said received video signal.

8. A video camera arranged in operation to produce a video signal representative of an image formed within a field of view of said camera, said video camera having an image processor as claimed in Claim 1 to which said video signal is fed, said image processor being arranged in operation to produce an output video signal by interpolating features of said image having at vertical and horizontal component.

9. A method of processing an image represented by a received video signal, said method producing an interpolated video signal from said received video signal, said method comprising the steps of

- identifying a feature in said image having a component in both a horizontal and a vertical dimensions,

- identifying the pixels associated with each of the horizontal lines of the video signal,

- for each of said horizontal lines storing a plurality of said input pixels, and

- generating an output video signal by selectively interpolating said stored plurality of input pixels associated with said feature to generate said interpolated video signal.

10. A computer program providing computer executable instructions, which when loaded onto a computer configures the computer to operate as an image processor as claimed in Claim 1.

11. A computer program providing computer executable instructions, which when loaded on to a computer causes the computer to perform the method according to Claim 9.

12. A computer program product having a computer readable medium and having recorded thereon information signals representative of the computer program claimed in Claim 10.